International Journal of Engineering Sciences Paradigms and Researches (IJESPR)
Vol. 48, Issue 01, Quarter 01 (January-February-March 2019)
Publishing Date: 18th March, 2019
(An Indexed, Referred, Peer Reviewed and Impact Factor Journal)
ISSN (Online): 2319-6564
www.ijesonline.com

VHDL Implementation of a Multiply Accumulate Unit (MAC) using reversible

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Abstract

In today's world technological advancements can be seen in each and every field. More and more technologies with lot of features and advantages are arising. Reversible logic is one such emerging concept. One of the main characteristic of reversible circuits is their less power consumption. As the technology improves, the number of components and hence the number of transistors packed on to the chip also increases. This causes increase in power consumption. Hence reduced power consumption of reversible logic has adequate importance in the present scenario. Reversible logic has a wide application in low power VLSI circuits. This paper presents the implementation of a reversible logic MAC unit and the design is done using Fredkin gate.

Keywords: *VHDL, MAC, Reversible Logic.*

I. Introduction

One of the important problems faced in electronic circuit designing is the energy dissipation. So the need for low power circuits and devices are growing day by day. The concept of reversible logic can be considered as a solution for the increase in power consumption of the electronic circuits. It was in 1961 that R. Landauer had introduced the concept of reversible computational logic. According to Landauer whenever there occurs a loss of one bit of information then a small amount of heat will be dissipated and would be equal to kTln2where 'k' is the Boltzman constant and T is the operational temperature[1]. Later, Bennett [2] proved that the energy kTln2 could be saved when the reversible circuitsare used. Reversible logic circuits are thosecircuits which are having a one to one correspondence between its inputs and outputs. Reversible logic gates are having the same number of inputs as well as outputs. For each input given to the reversible gates there would be a distinct output assignment. So inputs of the reversible gates can be uniquely found from its respective outputs.

Multipliers are one of the important element that determines a system's performance because the multiplier is the slowest element in the system. Hence, optimizing the speed and area of the multiplier is a major design issue. So implementing multipliers in reversible logic has utmost importance.In this paper a multiplier using AND arrays and a MAC unit using this multiplier have been synthesized using reversible gates. Fredkin gate is used for implementing the proposed design. This paper is organized in the following way: Section II describes about reversible logic and section III describes about some basic reversible logic gates. In section IV, implementation of certain logic functions using reversible gate is done. Section V deals with the implementation of certain systems using reversible logic.

II. Reversible Logic

A circuit/gate is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments.

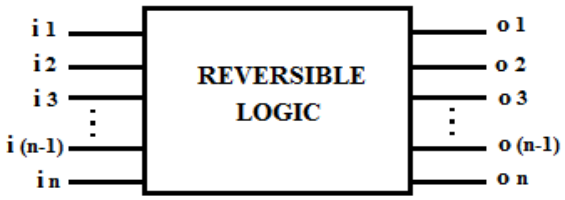

Figure 1: Reversible logic

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An N*N reversible gate can be represented as:

I=(i1,i2,i3,……in)

O=(o1,o2,o3,…….on)

Where I and O represent the input and output vectors respectively.

The number of input and output lines should be same in a reversible logic. All the reversible gates should run in both directions. This means that all the inputs can be recovered back from their corresponding outputs. Some of the parameters that determine the characteristics of reversible logic include number of reversible gates, number of constant inputs, garbage outputs etc. The number of inputs that should be put constant either at 0 or 1 for synthesizing the given logical function is called the constant inputs. Garbage output is defined as the number of unused outputs seen in a reversible circuit.

III. Commonly used Reversible Logic Gates

Several reversible logic gates have been proposed over the years. The simplest of all the reversible gates is NOT gate. It is a 1x1 gate. An example for 2x2 gate is Controlled NOT (CNOT) gate. Fredkin gate, Toffoli gate etc are some of the prominent 3x3 reversible gates.

A. NOT Gate

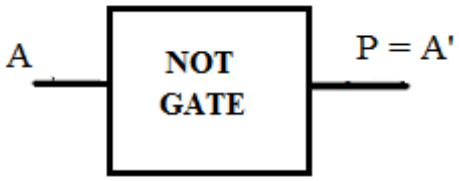

Figure 2: NOT Gate

At present NOT Gate is the only reversible gate which is commonly used. It is the only reversible gate among the conventional logic gates. It is a 1x1 gate.

B. CNOT Gate

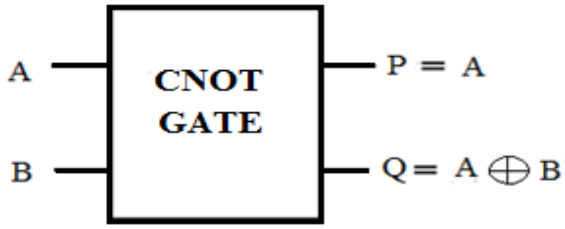

Figure 3: CNOT Gate

It is also called Feynman gate. It is a two input two output reversible gate having the mapping (A,B) to (P=A,Q=A xor B) where A, B are the inputs and P, Q are the outputs respectively.

C. Toffoli Gate

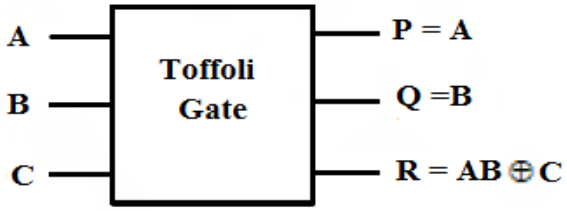

Figure 4: Toffoli gate

It is also known as the "controlled-controlled-not" gate, which describes its action. It has 3-bit inputs and outputs; if the first two bits are set, it inverts the third bit, otherwise all bits stay the same.

D. Fredkin Gate

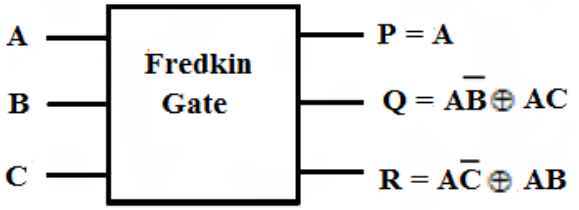

Figure 5: Fredkin Gate

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It is a 3x3 reversible gate. It is a three input three output reversible gate having the mapping (A, B, C) to (P = A, Q = AB⊕ AC , R = AC ⊕ AB).

IV. Implementation of Certain Logic Functions using Fredkin Gate

Logic functions like AND, OR, XOR etc can be implemented using reversible gates. In this paper the focus is mainly given to functions implemented using fredkin gates.

The FG can be used to create the inverse and signalduplication (fan-out) functions. Fig 6 is the Fredkin gate representation of the NOT function.

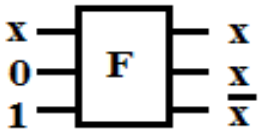

Figure 6: Fredkin gate implementation of NOT

Two input AND gate function can be implemented in reversible logic by grounding the third input of fredkin gate. Also a two input OR gate function can be generated by tying the third terminal of a fredkin gate to Vcc. Figure 7 shows the AND and OR implementation of fredkin gate.

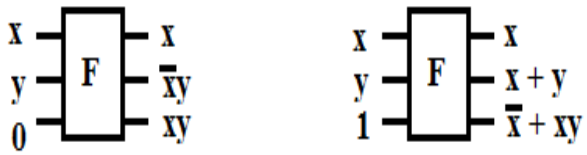

Figure 7: Implementation of AND and OR function using fredkin gate

A two input XOR function can be implemented by connecting two fredkin gates as shown in figure 8.

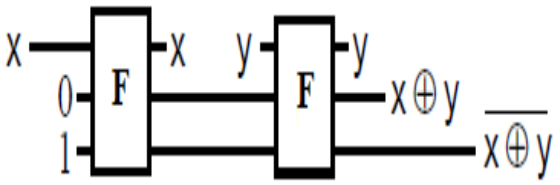

Figure 8: Implementation of XOR function using fredkin gate

Adders are the basic building blocks of many computation systems like multipliers. Adders can also be implemented using reversible gates. The simplest among the adders is the ripple carry adders. In ripple carry adders, full adders are connected in series to generate the sum and carry. A full addercomputes the sum bit s_i and the carry output c_{i+1} based on inputs a and b and carry input c. The output expressions for aripple carry adder are:

s_i = a xor b xor c;
c_{i+1} = ab + bc + ca;

A ripple carry adder using reversible gate is proposed in [3]. There the ripple carry adders are implemented using fredkin gate.
The worst case occurs in the ripple carry adder when the carry generated initially ripples through all the stages to reach the final stage.

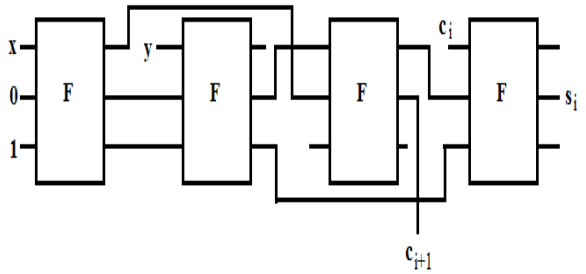

Figure 9: Full adder using fredkin gate

V. Proposed Works

A. Multiplier Using AND arrays

In this paper implementation of a multiplier with AND arrays is done using Fredkin gate. In this multiplier

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shift and add method is used.So this type of multiplier circuitry consists of circuits required for shifting as well as addition. The block diagram of multiplier using AND an array is shown in figure 10.

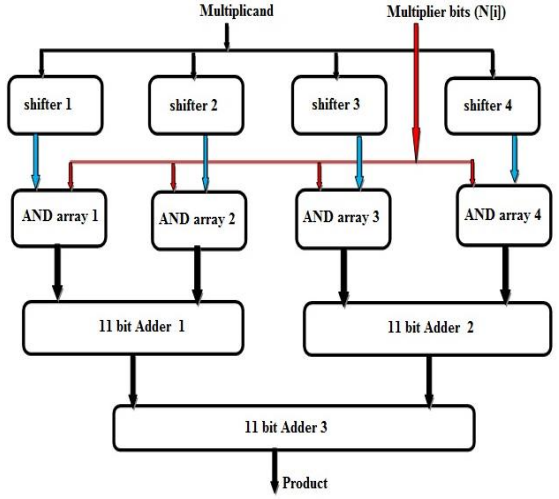

Figure 10: Block Diagram of multiplier

The steps done in this multiplier includes:

1. Shifting the Multiplicand. The number of times shifting is done according to the number of bits in multiplier.

2. Each shifted result of the multiplicand is multiplied by the corresponding bits of the multiplier.This is done using AND arrays.

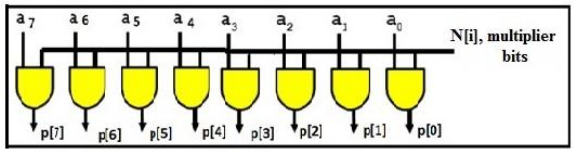

Figure 11: AND arrays

3. The result of each AND arrays is added together to get the final product.

B. Reversible Latches and Flip-flops

Flip-flops and latches are mainly used as data storage elements. Such data storage can be used for storage of state, and such a circuit is described as sequential logic. When used in a finite-state machine, the output and next state depend not only on its current input, but also on its current state. It can also be used for counting of pulses, and for synchronizing variably-timed input signals to some reference timing signal.

Flip-flops can be either simple or clocked (synchronous or edge-triggered); the simple ones are commonly called latches. The word latch is mainly used for storage elements, while clocked devices are described as flip-flops. A latch is level-sensitive, whereas a flip-flop is edge-sensitive.

Latches can be made using reversible gates. A Reversible D latch made using Fredkin gate [4] is shown in figure 12.

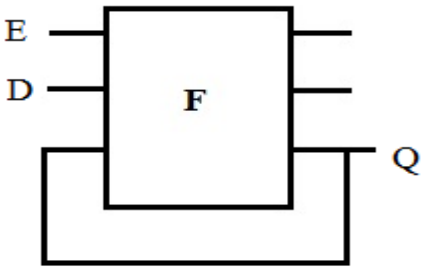

Figure 12: Reversible D-latch

Flip-flops are edge triggered. A negative edge triggered D flip-flop made using Fredkin gate is shown in figure 13. When the clock input is high the input is latched through the first fredkin gate to the input of the next gate. When the clock input is low, the second fredkin gate will latch the input value to its output. Thus the whole device acts as an edge-triggered flip-flop.

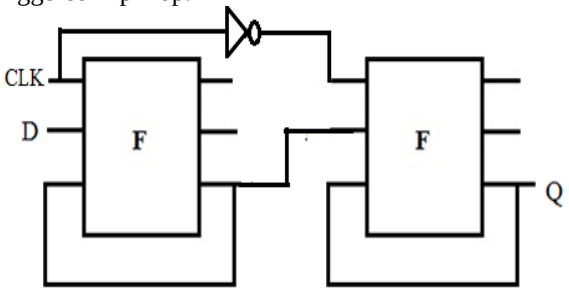

Figure 13: Reversible Edge triggered D flip-flop

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C. Reversible PIPO Shift Register

Shift registers are a type of sequential logic circuit, mainly for storage of digital data.For parallel in - parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits.The input bus provides the parallel inputs and the output bus gives the parallel outputs. Once the register is clocked, all the data at the D inputs appear at the corresponding Q outputs simultaneously.

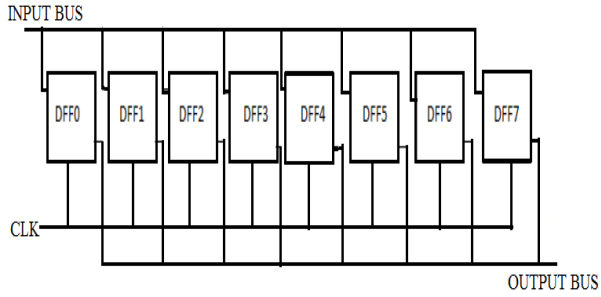

Figure 14: Reversible PIPO shift register

Here an eight bit PIPO register is made using the reversible D flip-flops shown above.

D. Reversible MAC unit

The multiply–accumulate operation is a common step that computes the product of two numbers and adds that product to an accumulator. The hardware unit that performs the operation is known as a multiplier–accumulator (MAC, or MAC unit); the operation itself is also often called a MAC or a MAC operation.Modern computers may contain a dedicated MAC, consisting of a multiplier implemented in combinational logic followed by an adder and an accumulator register that stores the result. The output of the register is fed back to one input of the adder, so that on each clock cycle, the output of the multiplier is added to the register. Combinational multipliers require a large amount of logic, but can compute a product much more quickly than the method of shifting and adding typical of earlier computers. The first processors to be equipped with MAC units were digital signal processors, but the technique is now also common in general-purpose processors.

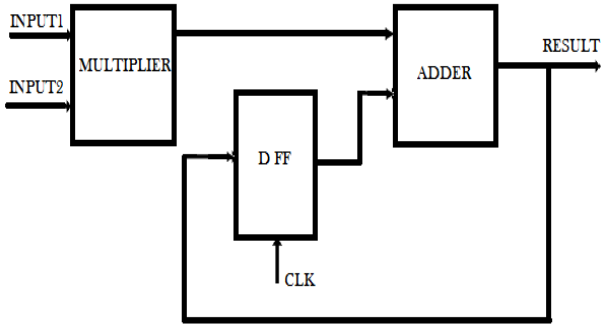

Figure 15: A MAC unit made using reversible components

A four bit MAC unit is proposed in this paper. It consists of a four bit multiplier using AND arrays made of reversible fredkin gate, an eleven bit reversible adder and a parallel in parallel out shift register made of reversible edge triggered D flip-flop. Here the input given to the system are first multiplied in the multiplier and the product is given to the adder, which adds the multiplier result with the previously stored result.

VI. Simulation Results

Mentor Graphics was the first to combine single kernel simulator (SKS) technology with a unified debug environment for Verilog, VHDL and SystemC. The combination of industry-leading, native SKS performance with the best integrated debug and analysis environment make ModelSim the simulator of choice for both ASIC and FPGA design. The best standards and platform support in the industry make it easy to adopt in the majority of process and tool flows. It has a unified mixed language simulation engine for ease of use and performance. It provides powerful waveform compare for easy analysis of differences and bugs. Output waveforms obtained in the simulation process using Modelsim are as follows:

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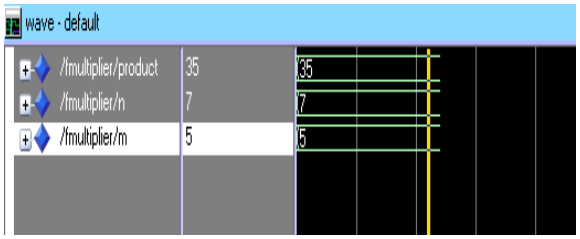

Figure 16: Output of reversible multiplier using AND arrays

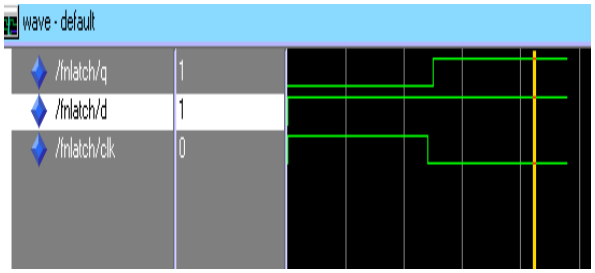

Figure 17: Output of reversible edge triggered flip-flop

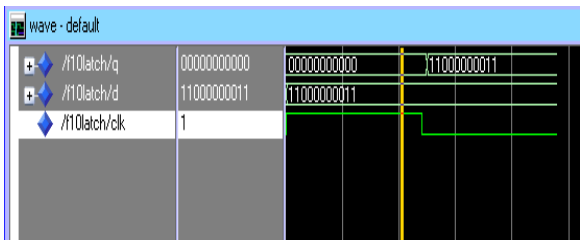

Figure 18: Output of reversible PIPO shift register

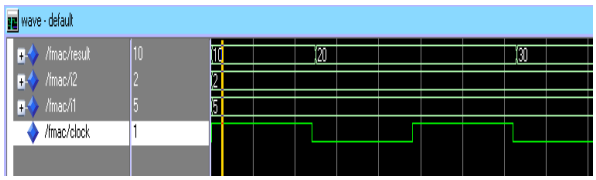

Figure 19: Output of reversible MAC unit

VII. Conclusion

This paper provides an insight into the introduction of the reversible logic technology. In this paper VHDL implementation of a multiplier with AND array is done using reversible gate.Multipliers are key components of many high performance systems such as FIR filters, microprocessors, digital signal processors etc. A system's performance is generally determined by the performance of the multiplier because the multiplier is the slowest element in the system. This paper also deals with a MAC unit implemented using reversible Fredkin gate. Loss of power is a major of concern of the present day circuits. Reversible logics and reversible circuits are providing the researchers a platform for analyzing and reducing the power consumption of a circuit.

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